GE Fanuc Automation

Programmable Control Products

Rx3i
Programmable Controller
Guide Form Specification

February 2004

1. GENERAL

1.1. SCOPE

1.1.1. This specification covers the technical requirement for a programmable controller which can receive discrete and analog inputs. Through the use of relay ladder logic and other IEC languages, including "C". The unit can control discrete and analog output functions, perform data handling operations and communicate with external devices.

2. MANUFACTURER'S QUALIFICATIONS

2.1. MANUFACTURER'S STANDARDS

2.1.1. The manufacturer shall have shown high commitment to product, manufacturing and design process quality. It shall have attained ISO 9000:2000 registration.

2.2. DESIGN AND MANUFACTURE

2.2.1. The programmable controller and all of the corresponding components within the family of controller products shall be offered by a company who regularly manufactures and services this type of equipment.

2.2.2. All products shall be designed, manufactured, and tested in accordance with recognized UL, C-UL, CSA, IEC and CE mark industrial standards. The system shall be operational during and after testing. See tables on the following page for standards requirements.

AGENCY APPROVALS OVERVIEW		*Comments*
Quality Assurance in Design/ Development, Production, Installation & Servicing	**ISO9001**	Certification by Underwriters Laboratories and BSI Quality Assurance
Safety for Industrial Control Equipment	**UL508**	Certification by Underwriters Laboratories
	C-UL or CSA22.2, 142-M1987	Certification by Underwriters Laboratories [C-UL] or Canadian Standards Association for selected modules
Safety for Hazardous Locations Class I, Div II, A, B, C, D	**UL1604 with C-UL**	Certification by Underwriters Laboratory for selected modules
	FM3611	Certification by Factory Mutual for selected modules
	CSA22.2, 213-M1987	Certification by Canadian Standards Association for selected modules
European EMC and Low Voltage Directives	**CE Mark**	Certification by Competent Body for EMC Directive for selected modules

STANDARDS OVERVIEW		*Conditions*
ENVIRONMENTAL		
Vibration	**IEC68-2-6, JISC0911**	1G @40-150Hz, 0.012in p-p @10-40Hz
Shock	**IEC68-2-27, JISC0912**	15G, 11ms
Operating Temperature		0°C to 60 °C:[inlet] 0°C to 55 °C:[ambient]
Storage Temperature		–40 ° C to +85 ° C
Humidity		5% to 95%, non-condensing
Enclosure Protection	**IEC529**	Steel cabinet per IP54: protection from dust & splashing water
EMC EMISSIONS		
Radiated, Conducted	**CISPR11, EN55011 FCC**	Class A [applies to CE Marked modules] part 15, subpart J, Class A
EMC IMMUNITY		**[applies to CE Marked modules]**
Electrostatic Discharge	**IEC 1000-4-2**	8KV Air, 4KV Contact
RF Susceptibility	**IEC 1000-4-3**	10V_{rms} / m 80Mhz to 1000Mhz, 80% AM
Fast Transient Burst	**IEC 1000-4-4**	2KV: power supplies, 1KV: I/O, communications
Surge Withstand	**ANSI/IEEE C37.90a**	Ring Wave, 2.5KV: power supplies, I/O [V2240V]
	IEC255-4	Ring Wave, Class II: power supplies, I/O [V2240V]
Conducted RF	**IEC 1000-4-6**	10V_{rms}, 150khz to 80Mhz, 80% AM: communication modules with cables >30m
ISOLATION		
Dielectric Withstand	**UL508, UL840, IEC664**	1.5KV for modules rated from 51v to 250v
POWER SUPPLY		
Input Dips, Variations	**IEC1000-4-11**	During Operation: Dips to 30% and 100%, Variation for AC + / - 10%, Variation for DC + / - 20%

2.2.3. The manufacturer shall have a fully operational quality assurance and quality control program in place and shall comply with ISO9001 standards for "Quality Systems- Model for Quality Assurance in Design/Development, Production, Installation, and Servicing."

2.2.4. Complete documentation describing installation, operation, programming and simple field maintenance shall be available in paper format and on CD-ROM.

2.3. SUPPORT

2.3.1. The manufacturer or its authorized representative shall provide complete global technical support for all of the products. This shall include headquarters or local training, regional application centers, and local or headquarters technical assistance. A toll-free (800) number hot-line shall be available for emergency support.

2.3.2. Product shall have a warranty period of at least 1 year from the date of purchase and an optional extended warranty.

3. PRODUCT

3.1. HARDWARE

3.1.1. GENERAL

3.1.1.1. The system shall consist of rugged components designed specifically for industrial environments. A complete system shall consist of one or more racks containing I/O modules, interconnected by signal cables.

3.1.2. PACKAGING

3.1.2.1. All components shall be housed in structurally secure enclosures.

3.1.2.2. The controller CPU shall be modular. It shall be fully enclosed within a durable plastic shroud. When mounted on the system base, the modular CPU shall not occupy more than two available slot.

3.1.2.3. The I/O system shall be modular. Each module shall be fully enclosed within a durable plastic shroud. When mounted on the system base, each I/O module shall not occupy more than one available slot. Loops shall be part of the module for securing field wiring.

3.1.2.4. There shall be at least two sizes of I/O bases available. One shall hold up to 12 I/O modules and the other shall hold up to 16 I/O modules. The base shall support a high speed serial bus and a high speed PCI bus.

3.1.2.5. I/O modules shall be retained in their slot by a hinge on the upper rear edge and snap on the lower rear edge of the baseplate. Removing the module shall require no tools.

3.1.2.6. I/O modules shall be installed in any available slot in the CPU or expansion baseplates, and shall require no tools for insertion and extraction.

3.1.2.7. I/O modules shall connect electrically to the baseplate via a pin and socket connector.

3.1.2.8. I/O modules shall be fully enclosed in a plastic covering protecting the electronic circuitry from exposure.

3.1.3. DURABILITY

3.1.3.1. All components within the controller family shall be manufactured with a high degree of durability.

3.1.3.2. All switches and other operator-controlled devices shall be of the size and durability for the intended use as is normally offered for industrial applications.

3.1.3.3. All signal cables furnished by the manufacturer shall be constructed so as to withstand, without damage, all normal use and handling.

3.1.4. PARTS INTERCHANGE

3.1.4.1. In order to minimize spare parts stocking requirements, the controller family shall have a high degree of interchange capability. The power supply, battery, EEPROM Chips should all operate equally well regardless of the CPU being used.

3.1.4.2. The system shall incorporate a modular design using plug-in assemblies with pin and socket connectors.

3.1.4.3. Wherever possible, all assemblies and sub-assemblies performing similar functions shall be interchangeable.

3.1.4.4. The system design shall accommodate the replacement of assemblies without having to disconnect field wiring. Wherever possible, removable connectors shall be used to connect field wiring to the individual circuit board assemblies.

3.1.4.5. All major assemblies and sub-assemblies, circuit boards, and devices shall be identified using permanent labels or markings each of which indicates the manufacturer's catalog number, product manufacturing date code, UL and C-UL certifications.

3.2. ENVIRONMENTAL CONDITIONS

3.2.1. GENERAL

3.2.1.1. All components of the controller system, except CRT terminals and programming workstations, shall meet the following environmental specifications:

3.2.2. STORAGE CONDITIONS:

TEMPERATURE -40 to 85 degrees Celsius

3.2.3. OPERATING CONDITIONS:

TEMPERATURE 0 to 60 degrees Celsius

3.2.4. HUMIDITY:

5 to 95% relative humidity, non-condensing

3.3. POWER SUPPLY

3.3.1. TYPES OF POWER SUPPLY

3.3.1.1. The power supply shall be one of two types:

- Type 1: High Voltage, High Capacity AC/DC

A wide range supply operating from a voltage source in the range of 180 to 264 VAC and 90 to 125 VDC, providing 40 Watts of power. The power supply shall be mo more than two modules wide.

- Type 2: Low Voltage, High Capacity DC

  A DC power supply operating from a 12 VDC to 30 VDC voltage source. provide 40 Watts of power. Power supply shall be a single wide module.

3.3.2. SPECIFICATIONS

3.3.2.1. The power supply shall contain internal diagnostics to detect over temp and over load conditions.

3.3.2.1. LEDs on the power supply shall indicate over temp and over load. This diagnostic information will also be available to the CPU.

3.3.2.2. The power supply shall support hot insertion.

3.3.2.3. Multiple power supplies shall be supported on the base to support redundant power supplies or for more capacity.

3.3.2.4. The power supply shall be modular in design, separate from the CPU and baseplate for easy replacement in the unlikely event of failure.

3.3.2.5. The power supply shall have a ON/OFF switch

3.4. CENTRAL PROCESSING UNIT (CPU)

3.4.1. TYPES OF CPU

3.4.1.1. The CPU shall be offered, a modular type. The CPU shall possess the capability to solve application logic, store the application program, store numerical values related to the application processes and logic, and interface to the I/O systems. The CPU shall need no additional modules to provide at least the following advanced programming features: Floating Point Math, PID, Modulo, Math, Double Precision math, Logical functions, Subroutines, Data Array Move and Indirect Addressing.

3.4.2. MODULAR CPU

3.4.2.1. The modular type CPU shall contain: A minimum Intel Pentium microprocessor operating at speeds no less than 300 MHz as the main processing element, memory mounted on the board. A minimum of 10Megbytes of memory shall be on board for user configurable application, data storage and documentation storage.

3.4.2.2. The modular type CPU shall contain a real-time calendar and clock that can be accessed by the user program. This Time of Day clock and calendar shall be battery-backed and maintain seven time functions: Year (2 digits), Month, Day of Month, Hour, Minute, Second, and Day of week.

3.4.2.3. The modular CPU shall execute Boolean functions at a rate of 0.3 microseconds per instruction or lower.

3.4.2.4. The modular CPU shall be capable of controlling up to 79 I/O slots.

3.4.2.5. The modular CPU shall be able to provide special functions such as High Speed Counter function, Axis Positioning function, and Local Area Networking function.

3.4.2.6 The CPU shall be able to provide 2 serial ports, 1 9 pin RS232 and 1 a 15 pin RS485 for communications.

3.4.2.7.1 The modular CPU shall contain a battery slot to support backup power for the SRAM

3.4.2.7.2 A RUN ENABLED/RUN DISABLED/STOP switch shall be on the CPU behind a door for security.

3.4.2.7.3 LEDs on the CPU shall indicate the following:

- CPU OK
- RUN mode
- Outputs Enabled
- I/O Force

- Battery condition
- System faults
- Comm 1 activity
- Comm 2 activity

3.5. SYSTEM DIAGNOSTICS

3.5.1. VISUAL DIAGNOSTICS

3.5.1.1. Status of low or dead battery shall be indicated by a red Battery LED on the power supply module.

3.5.1.2. The diagnostic status of the fuses, for those discrete I/O modules containing fuses, shall be indicated by a red LED mounted on the top of the module. The red LED shall illuminate when a blown fuse condition is present.

3.5.2. ALARM PROCESSOR

3.5.2.1. The CPU shall contain an alarm processor that is special PAC feature designed to receive and process faults. The diagnostics shall provide information on the configuration and CPU, memory, communications and I/O status.

3.5.2.2. The alarm processor function shall log I/O and system faults in two fault tables that shall be accessible for display on the PC compatible programming software screen or uploaded to a host computer or other coprocessor.

3.5.2.3. The alarm processor shall maintain the states of up to 128 discrete system diagnostic bits to be read by a host or incorporated as contacts into the ladder program for customized diagnostic routines.

3.5.2.4. Each fault table shall have a total capacity of 32 faults. The last 16 entries shall maintain the latest 16 faults. The first 16 shall be kept unchanged.

3.5.2.5. Faults may be cleared by the user by way of a programmer. Provision shall be made by way of passwords to protect these faults from unauthorized clearing.

3.5.3. ALARM FEATURES

3.5.3.1. The alarm processor shall report three types of fault action; fatal, diagnostic, or informational, and the CPU shall respond as follows:

FAULT ACTION	FATAL	DIAGNOSTIC	INFORMATIVE
CPU Enters STOP Mode	YES	NO	NO
Set Diagnostic Bit	YES	YES	NO
Logged In Fault Table	YES	YES	YES

3.5.3.2. When an I/O fault occurs, the alarm processor shall report the rack and slot location of the fault, the condition, the address and the circuit number if appropriate.

3.5.3.3. When modular CPU is used, this alarm processor function shall have the capability to time-stamp system faults for future references.

3.6. SYSTEM SECURITY

3.6.1. PAC MEMORY PROTECTION

3.6.1.1. The PAC shall have 4 levels of security or password privilege levels to prevent unauthorized changes to the contents of the PAC. These built-in privilege levels shall be set in the programming software or with the Hand-Held Programmer and shall impose the following constraints:

Level	Constraint
1	Read PAC data only (except passwords)
2	Write to any data memory
3	#2 and write to all configuration or logic in STOP mode
4	#3 and write to logic in STOP or RUN mode (on-line change) and password level access.

3.6.1.2. There shall be one password, one to four ASCII characters in length, for each privilege level in the PAC, and the same password can be used for more than one level.

3.6.1.3. Any attempts to access or modify information in the PAC without the proper password privilege level shall be denied.

3.6.2. SUBROUTINE PASSWORD

3.6.2.1. The PAC shall have a software OEM key that allows users to control access to each subroutine in the relay ladder program.

3.6.3. OEM PROGRAM PROTECTION

3.6.3.1. The PAC shall have a software OEM key that allows users to protect the resident program from unauthorized reads and writes.

3.7. CPU MEMORY

3.7.1. MEMORY CAPACITY

3.7.1.1. The PAC shall supply a modular design CPU that contains at least the following:

- 10Megbytes for application programming
- Configurable up to 5Meg 16-bit registers for register and data usage
- Up to 32K control relays internal battery backed
- Up to 32K bits for discrete inputs
- Up to 32K bits for discrete outputs
- Configurable up to 32K 16-bit registers for analog inputs
- Configurable up to 32K 16-bit registers for analog outputs

3.7.1.2. All application memory shall be available to the user program. Executive level operations performed by the CPU shall not consume application memory.

3.7.2. MEMORY STORAGE

3.7.2.1. The register values and the application program shall be stored in battery backed, SRAM. The application program and system configuration shall also be stored in FLASH memory if so selected.

3.7.2.2. There shall be a long-life Lithium battery used to maintain the contents of the CMOS RAM memory in the CPU.

3.7.2.3. There shall be an easily accessible battery compartment in the power supply with dual battery connectors. The battery shall be replaceable with power applied to the PAC and without removing the CPU.

3.7.2.4. An LED shall provide visual indication of the battery condition. Additionally, a low battery condition shall be alarmed with a system diagnostic bit.

3.7.2.5. The CPU shall allow resident user program to be maintained in the CPU without power applied. Two levels of maintainability shall be provided, short duration and long duration.

3.7.2.6. For short duration, the program shall be maintained by a hi-capacity capacitor for a period of no less than 1 hour. This allows adequate time for replacing the battery in the power supply module, should the external supply to the CPU be interrupted.

3.7.2.7. For long duration, the CPU module shall maintain its contents by using the battery. This allows the CPU module to be shipped via surface mail where power supply to the module is not available. This method may be achieved by providing internally mounted battery. If the CPU module does not have an internal battery then an external battery board may be used.

3.7.2.8. The CPU shall calculate the application program checksum at the end of every sweep. A complete checksum calculation for a program may take several sweeps. A fixed number of program memory checksum shall be calculated each sweep. This number is configurable by the user. If the calculated checksum does not equal the reference checksum, a fault shall be recorded, and the CPU mode will change to STOP.

3.8. PROGRAMMING ENVIRONMENT

3.8.1. PROGRAMMING DEVICES

3.8.1.1. At least two programming devices shall be available for development of application programs, a small hand-held device with back-lit LCD readout and a Software programming package running on a PC compatible laptop or desktop computer.

3.8.1.2. On-line and off-line, CPU and I/O configuration and application program development shall be achieved with a PC compatible computer and programming and documentation software.

3.8.1.3. The PC compatible computer shall be connectable to the PAC via a built-in serial communication port.

3.8.1.4. In addition to the serial communications, the PC compatible computer shall be connectable to the PAC via Ethernet TCPIP supporting the SRTP application protocol. A separate module providing Ethernet communications through 10baseT connection.

3.8.1.5. The programming devices shall have access to the application program, the CPU and I/O system configurations, all registers, CPU and I/O status, system diagnostic relays, and I/O over-ride capabilities

3.8.5 OPERATOR INTERFACE

3.8.5.1 The programming port and its protocol shall be open in architecture. The protocols of this communication port shall be published such that a user may develop their own operator interface device, software or hardware, to access Register, I/O status, I/O override and system diagnostic memory data.

3.8.5.2 Through an open nature of this communications protocol, a wide variety of operator interface shall be made available. These may be manufacturer's own brand or they may be manufactured by 3rd party vendors.

3.9. INSTRUCTION SET

3.9.1. PROGRAMMING LANGUAGE

3.9.1.1. The CPU shall be capable of solving an application program whose source format shall be relay ladder diagram. The language shall support relay, timers and counters, arithmetic, relational, bit operation, data move, conversion, and control functions.

3.9.1.2. The CPU shall be capable of solving an application program whose main program format is in Sequential Function Chart (SFC) with underlying code in relay ladder diagram.

3.9.2. RELAY FUNCTIONS

3.9.2.1. Relay ladder operations shall consist of the following contacts and coils:

RELAY FUNCTIONS
Normally Open Contact
Normally Closed Contact
Coil
Negated Coil
Retentive Coil
Negated Retentive Coil
Positive Transition Coil
Negative Transition Coil
Set Coil (Latch)
Reset Coil (Unlatch)
Retentive Set Coil
Retentive Reset Coil

3.9.2.2. Positive transition coils and negative transition coils shall function as leading and trailing edge one-shot coils respectively.

3.9.2.3. Contacts may be referenced any number of times within the application program.

3.9.2.4. A single rung may contain more than one coil.

3.9.2.5. There shall be a service that allows user programs to be checked for multiple coil use. This flag may be set to:

- Disallow more than one coil in a single rung
- Allow multiple coil use but generate warning messages

- Allow multiple coil use without warnings

3.9.3. TIMERS AND COUNTERS

3.9.3.1. Timer and counter operations shall consist of the following types:

TIMERS AND COUNTER FUNCTIONS
Retentive On-Delay Timer (ONDTR)
Simple Off- Delay Timer (OFDT)
Simple On-Delay Timer (TMR)
Up Counter (UPCTR)
Down Counter (DNCTR)

3.9.3.2. The retentive on-delay timer shall behave as a stop-watch that increments time when enabled and holds the current timed value until receiving power flow to the reset input.

3.9.3.3. The simple on-delay timer shall increment while it receives power flow and reset to zero when power flow stops.

3.9.3.4. The simple off-delay timer shall increment while it power flow stops and reset to zero when power flow is present.

3.9.3.5. There shall be at least 10,666 programmed timers and/or counters available for use in application programs.

3.9.3.6. Each timer or counter requires the use of three 16-bit registers within %R memory for storage of the preset, the current value and a control word. These three registers shall be accessible to the user via a register reference.

3.9.3.7. The timers and counters shall not require an output reference, the output of a timer or counter can be used to energize a coil, or enable another function, such as a math function, or another timer or counter.

3.9.3.8. The time/count limit shall be either a programmed constant or shall be programmable via a register reference value.

3.9.3.9. The time shall be counted in tenths of seconds or hundredths of seconds, and the range for the timers and counters is 0 to 32,767 time units.

3.9.4. ARITHMETIC

3.9.4.1. The arithmetic operations shall support two data types, Signed Integer (INT), and Double Precision Integer (DINT). On the modular CPU, the Floating Point data type shall also be supported via floating point emulation. Arithmetic functions shall consist of the following types:

ARITHMETIC FUNCTIONS
Addition
Subtraction
Multiplication
Division (quotient)
Modulo (remainder)
Square Root

3.9.4.2. Signed Integers (INT) data shall be stored in 16 contiguous bits of memory, in 2's complement notation. The range for Signed Integer Data shall be -32,768 to +32,767.

3.9.4.3. Double Precision Integer (DINT) data shall be stored in 32 contiguous bits of memory, double precision data is always signed. The range for Double Precision Integer Data shall be -2,147,483,648 to 2,147,483,647.

3.9.4.4. The arithmetic function blocks shall consist of 3 inputs and 2 outputs. The enable input shall begin the execution. When the function is enabled, the two data inputs are operated upon and the result is output. There shall also be an OK output that is always true when the function is enabled, unless an overflow or other error exists.

3.9.4.5. All of the Arithmetic functions shall be such that they can be cascaded together in a single rung.

3.9.5. RELATIONAL FUNCTIONS

3.9.5.1. Relation Functions which are used to compare two numbers, shall operate on Signed Integer and Double Precision Integer data types, and shall consist of the following types:

RELATIONAL FUNCTIONS

Equal To	Not Equal To
Greater Than	Greater Than or Equal to
Less Than	Less Than or Equal to

3.9.6. BIT OPERATION FUNCTIONS

3.9.6.1. Bit Operation Functions shall perform comparison and movement operations on word data that is specified as a continuous string of data in 16-bit increments, with the first bit of the first word being the least significant bit, and the last bit of the last word being the most significant bit.

3.9.6.2. Bit Operation Functions that are used to perform Boolean operations on corresponding bits of two bit strings of the same length shall consist of the following types:

BOOLEAN FUNCTIONS
Logical AND
Logical OR
Logical Exclusive OR

3.9.6.3. Bit Operation Functions used to create an output string that is a copy of an input bit string, but with its bits inverted, shifted, or rotated shall consist of the following types:

BIT FUNCTIONS
Logical Invert (NOT)
Shift Left
Shift Right
Rotate Left
Rotate Right

3.9.6.4. The shift functions shall allow for the user to specify the number of places that the array is to be shifted as an input, and provide the state of the last bit shifted out, and a copy of the shift register as outputs.

3.9.7. DATA MOVE FUNCTIONS

3.9.7.1. Basic data movement capabilities shall be provided by the following list of functions:

DATA MOVE FUNCTIONS
Move
Block Move
Block Clear
Shift Register
Bit Sequencer
Drum Sequencer
Range
Communications Request

3.9.7.2. The movement of data (16 bit integer or word), as individual bits, from one location to another shall be accomplished by the Move function. The user shall be able to specify the length of the move.

3.9.7.3. The Block Move function shall provide the functionality to move a block of 7 constants (integer or word) to a specified location.

3.9.7.4. The ability to fill a specified block of data (word) with zeros shall be accomplished by the Block Clear function. The user shall be able to specify the length of the block.

3.9.7.5. The Shift Register function shall provide the functionality to shift one or more data words from a reference location into a specified memory location. All of the data within the Shift Register shall be accessible throughout the program from logic addressed memory.

3.9.7.6. A method of shifting a bit sequence through an array of bits shall be provided by a Bit Sequencer function. The function shall provide the ability to reset the sequence, change the direction of the bit pattern, or access the step location within the array.

3.9.7.7. A method of checking for a value to be contained within a group of values shall be provided in a Range function.

3.9.7.8. Provisions to initiate communications with a specialized communication module shall be made through the use of a Communication Request function. This function shall allow the PAC to behave as a master on a serial communication link, thus providing the ability to communicate master/slave or peer to peer with any controller or computer using the same serial communication protocol.

3.9.8. TABLE

3.9.8.1. Table operations shall consist of moving data into or out of tables and searching for data of values equal to, not equal to, greater than, greater than or equal to, less than and less than or equal to a specified value.

TABLE FUNCTIONS
Array moves
Search Equal
Search Not Equal
Search Greater Than
Search Greater Than or Equal to

Search Less Than
Search Less Than or Equal to

3.9.8.2. The array move feature shall be capable of implementing indirect addressing applications.

3.9.9. CONVERSION FUNCTIONS

3.9.9.1. Two conversion functions shall be provided to convert a data item from a 4 digit Binary Coded Decimal (BCD-4) data type to a 16 bit signed integer and vice versa.

3.9.10. CONTROL FUNCTIONS

3.9.10.1. Control functions shall be provided to limit program execution, alter the way the CPU executes the application program, or provide special PAC services. The following Control Functions shall be provided:

CONTROL FUNCTIONS
CALL
Immediate I/O update (DO I/O)
Comment rung (COMMNT)
Master Control Relay (MCR, END MCR)
Jump to a label (JUMP, LABEL)
Special Service Requests (SVCREQ)

3.9.10.2. An immediate I/O update function shall be provided for the update of all or a portion of the inputs or outputs for one scan while the program is running, or to update I/O during the program in addition to the normal I/O scan.

3.9.10.3. Additionally, the function shall provide a mean to read inputs into memory auxiliary to the true input table, and execute outputs from discrete memory alternate to the true output table.

3.9.10.4. A comment rung function shall be provided to enter a rung explanation in the program. The rung explanation shall have the capacity to hold 2048 characters of text. The memory required for the comment shall be independent of the program storage memory. The comment shall have the ability to be edited via the PC compatible programming software.

3.9.10.5. A master control relay function shall allow all rungs between the MCR and its subsequent END MCR function to be executed without power flow.

3.9.10.6. A method for structuring the ladder program shall be provided with the use of a JUMP Function. This will cause the program execution to jump to a specified location in the logic targeted by the location of the LABEL function.

3.9.10.7. Seven different special PAC service requests shall be accessible by the programmer by utilizing one of the Service Request Functions listed below:

SERVICE REQUEST FUNCTIONS
Change/Read Checksum Task State and
Logical Number of Words to Checksum
Change/Read Time of Day Clock.
Shut Down the PAC.
Clear Fault Tables.
Read Last Fault Table Entry.
Read Elapsed time Clock.
Read I/O Override Status.

3.9.10.8. The Data written by these service request functions shall be in BCD or Packed ASCII format, and written into user definable register locations.

3.9.11. PID FUNCTION

3.9.11.1. A single PID function block instruction must be provided by the CPU without any additional module. Two versions of this closed loop control algorithm (Proportional/Integral/Derivative) shall be available:

- The standard ISA PID algorithm, which applies the proportional gain to each of the proportional, derivative, and integral terms; and
- The independent algorithm that applies the proportional gain only to the proportional gain term.

3.9.12. SUBROUTINE FUNCTION

3.9.12.1. A single function block must be available to allow repetitive call of a function. A password to protect the integrity of the subroutine must also be available.

3.9.12.2. A Subroutine may be called from within another subroutine. The nesting must be at least 8 deep.

3.9.12.3. A Periodic Subroutine shall be available that is executed once a programmable interval. The interval shall be between 1 and 10 milliseconds. The accuracy of the subroutine execution shall be 50 nanoseconds. Discrete I/O shall be available to update during the execution of the subroutine.

3.10. DISCRETE I/O

3.10.1. MODULARITY

3.10.1.1. Interface between the PAC and user supplied input and output field devices shall be provided by rack type I/O modules.

3.10.2. CONFIGURATION

3.10.2.1. There shall be an expandable system.

3.10.2.2. An expandable I/O system shall be supported by a single slot modular CPU, and shall accommodate up to 8 total racks or 79 I/O slots up to a total distance of 50 feet with the standard expansion racks and 700 feet with the remote expansion racks.

3.10.2.3. Serial expansion I/O racks shall be connected to the CPU rack via a high speed serial interface cable. The receiver shall be contained within the expansion baseplates eliminating the requirement for additional communication modules.

3.10.2.5 Ethernet expansion racks shall be connected via a 10/100Mbs Ethernet, RJ-45 connection. The Ethernet network interface unit shall reside in the rack using the same I/O that is compatible with the controller. The Ethernet network interface unit shall support the following:

- Built-in switch to allow daisy chain connection to the next Ethernet network interface unit.
- Support redundant controllers with automatic switch over.
- Ethernet network interface unit shall support up to 79 I/O modules per drop with local expansion.

3.10.3. I/O ADDRESSING

3.10.3.1. I/O reference addressing for each I/O module shall be assigned through the use of the PC compatible configuration and programming software or the hand held programmer. There shall be no jumpers or DIP switch settings required to address modules.

3.10.3.2. The circuit status of each I/O point on a module shall be indicated by a green LED mounted at the top of the module. These LED's must be visible through a clear plastic lens. Each LED shall illuminate a letter and number which corresponds to the energized I/O circuit.

3.10.3.3. Addressing of all references including I/O must be represented as a Decimal Based number.

3.10.4. CONSTRUCTION

3.10.4.1. Terminal blocks shall be easily removable, and common to all discrete and analog I/O to allow for convenient pre-wiring of field devices.

3.10.4.2. Each I/O module shall contain a hinged, clear plastic, terminal block cover (door) with a removable label.

3.10.4.3. The inside of the label shall have the module description, catalog number, and circuit wiring diagram for that module type, and the outside of the label shall have a user legend space to record circuit identification information.

3.10.4.4. The label shall have color coding for quick identification of the module as high voltage (red), low voltage (blue), or signal level (gray) type.

3.10.5. ELECTRICAL SPECIFICATIONS

3.10.5.1. I/O modules shall be designed for 1500 volt isolation between the field wiring and the system backplane.

3.10.6. INPUT SPECIFICATIONS

3.10.6.1. The 120 Volt AC input module shall accommodate an input voltage range from 0 to 132 volts.

3.10.6.2. The 240 Volt AC input module shall accommodate an input voltage range from 0 to 264 volts.

3.10.6.3. The 24 Volt DC positive and negative logic input modules shall accommodate an input voltage range of 0 to +30 volts DC.

3.10.6.4. The 125 Volt DC input module shall accommodate an input voltage range from 0 to 150 volts.

3.10.7. AVAILABILITY OF INPUT MODULES

3.10.7.1. As a minimum, the following discrete input modules shall be available:

Description	Points/Module
Input Simulator	8, 16
120 Vac Isolated Input	8
240 Vac Isolated Input	8
120 Vac Input	16
48Vdc Positive/Negative Logic Inpu	16
24 Vac/Vdc Negative Logic Input	16
24 Vdc, Positive/Negative Logic Input	8.16.32
24 Vdc Positive/Negative Logic Input, (1ms response)	16
125 Vdc Positive/Negative Logic Input	8
5/12 Vdc Positive/Negative Logic Input (TTL)	32

3.10.8. OUTPUT SPECIFICATIONS

3.10.8.1. Discrete AC output modules shall have separate and independent commons allowing each group to be used on different phases of AC supply.

3.10.8.2. Each discrete AC output shall be provided with an RC snubber to protect against transient electrical noise on the power line.

3.10.8.3. Discrete AC outputs shall be suitable for controlling a wide range of inductive and incandescent loads by providing a high degree of inrush current (10x the rated current).

3.10.8.4. Discrete DC output modules shall be available with positive and negative logic characteristics in compliance with the IEC industry standard.

3.10.8.5. Discrete DC output modules shall be provided with at least eight output points in a group with a common power input terminal per group.

3.10.8.6. Discrete DC output modules shall be compatible with a wide range of user-supplied load devices, such as: motor starters, solenoids, and indicators.

3.10.8.7. A 2 Amp relay output module shall be capable of supplying 2 Amps resistive maximum load per output and 4 amps resistive maximum load per group of 4 outputs.

3.10.8.8. A 4 Amp relay output module shall have 8 isolated outputs per module and shall be capable of supplying 4 amps resistive maximum load per output and 32 amps resistive maximum load per module.

3.10.9. AVAILABILITY OF OUTPUT MODULES

3.10.9.1. As a minimum, the following discrete output modules shall be available:

Description	Points/Module	Fuse Rating	# Fuses/ Module
120 VAC, 0.5A (2 groups)	12,16	3A	2
120/240 VAC, 1A (2 groups)	8	3A	2
120/240 VAC Isolated, 2A	5	3A	5
48VDC Positive Logic, 0.5A	8	0.5A	2
12/24 VDC Positive Logic, 2A	8	5A	2
12/24 VDC Positive Logic, 0.5A	8.16,32	N/A	0
12/24 VDC Negative Logic, 2A	8	5A	2
12/24 VDC Negative Logic, 0.5A	8,16	N/A	0
125 VDC Positive/Negative Logic, 1A	6	N/A	0
5/12/24 Vdc Negative Logic, 0.5A	32	N/A	0
Relay, Normally Open, 2A (4 groups)	16	N/A	0
Relay, Normally Open, 4A Isolated	8	N/A	0
Relay, Isolated, 4 Normally Closed, Normally Open (Form B & C) 8A	8	N/A	0
Solenoid Valve Output (Pneumatic)	11	100 psi	0

3.10.10. AVAILABILITY OF MIXED I/O MODULES

3.10.10.1. As a minimum, the following discrete output modules shall be available:

Description	Points/Module
24 Vdc Input, Relay Output	8 in, 8 out
120 Vac Input, Relay Output	8 in, 8 out

3.11. ANALOG I/O

3.11.1. GENERAL SPECIFICATIONS

3.11.1.1. For the conversion of analog to digital and digital to analog conversion required by an application, the following shall be available:

3.11.2. ANALOG VOLTAGE INPUT

3.11.2.1. The analog voltage input module shall be capable of converting 4 or 16 channels of inputs in the range of -10 to +10 volts.

3.11.2.2. Resolution of the converted analog voltage input signal shall be 12 bits binary or 1 part in 4096.

3.11.2.3. All of the channels of converted analog voltage input signals shall be updated each scan into a dedicated area of data registers in a 16-bit 2's complement format.

3.11.2.4. The conversion speed for all of the analog voltage input channels shall be no less than 2 milliseconds and no greater than 13 milliseconds..

3.11.2.5. The analog voltage input module shall be configurable to a 4 to 20 mA analog current input via an external resistor.

3.11.3. ANALOG CURRENT INPUT

3.11.3.1. The analog current input module shall be capable of converting 4 or 16 channels of inputs in the range of 4 to 20 mA or 0 to 20 mA.

3.11.3.2. Resolution of the converted analog current input signal shall be 12 bits binary or 1 part in 4096.

3.11.3.3. All of the channels of converted analog current put signals shall be updated each scan into a dedicated area of data registers in a 16-bit 2's complement format.

3.11.3.4. The conversion speed for all analog current input channels shall be a minimum of 2 milliseconds and no greater the 13 milliseconds.

3.11.4. ANALOG VOLTAGE OUTPUT

3.11.4.1. The analog voltage output module shall be capable of converting 2 or 8 channels of digital data to analog outputs in the range of -10 to +10 volts.

3.11.4.2. Resolution of the converted output signal shall be 13 bits or 16 bits.

3.11.4.3. All channels of analog output data shall be updated each scan from a dedicated area of data registers in a 16-bit 2's complement format.

3.11.4.4. The analog voltage outputs shall be configurable to default to 0 mA, 4 mA or hold-last-state in the event of a CPU failure.

3.11.5. ANALOG CURRENT OUTPUT

3.11.5.1. The analog current output module shall be capable of converting 2 or 8 channels of digital data to analog outputs in the range of 0 to 20 mA. .

3.11.5.2. Resolution of the converted output signal shall be 12 bits or 16 bits.

3.11.5.3. All channels of analog output data shall be updated each scan from a dedicated area of data registers in a 16-bit 2's complement format.

3.11.5.4. The analog current outputs shall be configurable to default to 0 volts or hold-last-state in the event of a CPU failure.

3.11.6. ANALOG COMBINATION

3.11.6.1. The analog combo module shall be capable of converting 4 channels of analog inputs to digital data and 2 channels of digital data to analog outputs.

3.11.6.2. All channels are configurable for 0-20ma, 4-20ma, 0-+10V, and -10-+10V. Resolution of the converted input signals shall be 12 bits and output signals shall be 16 bits.

3.11.6.3. All channels of analog data shall be updated each scan from a dedicated area of data registers in a 16-bit 2's complement format.

3.11.6.4. The analog outputs shall be configurable to default to 0 volts or hold-last-state in the event of a CPU failure.

3.11.7. MODULE AVAILABILITY

As a minimum, the following analog modules shall be available:

Description	Channels/Module
Input	4, 16
Voltage Analog Input	4, 16

Current Analog Output	2, 8
Voltage Analog Output	2, 8
Universal V, C, RTD, TC, Strain	8
Combo Analog Inputs/Outputs	4/2

3.12. SPECIALTY MODULES

3.12.1. TEMPERATURE CONTROL MODULE

3.12.1.1. A specialized temperature control module shall be available to accommodate applications where precise temperature control is needed.

3.12.1.2. The temperature control module shall support auto-tuning, closed looped PID control, and open looped manual control.

3.12.1.3. The temperature control module shall provide eight thermocouple inputs, 1 RTD input, and 8 PID-controlled output channels for controlling heaters.

3.12.1.4. The temperature control module shall provide alarms indications for each status zone, voltage failure, open or reversed thermocouple, compensation temperature error, high or low temperature, high or low temperature deviation, and open channel short circuit.

3.12.2. MOTION CONTROL

3.12.2.1. Specialized analog and digital motion control modules shall be available to perform 4 axes of closed or open loop servo control. These modules shall support encoder feedback with analog (up to 4 axis) or digital (up to 2 axis) output for velocity command.

3.12.2.2. The positioning mode shall support linear and S curve acceleration and deceleration.

3.12.2.3. The modules shall provide user-defined control inputs and outputs for application such as torque follower and flying cut-off applications.

3.12.2.4. The modules must have user defined inputs and outputs, an English-language programming software, and automatic data transfer of data between PAC and axis positioning module with no user programming.

3.12.2.5. The positioning mode shall have a powerful instruction set, that includes absolute or incremental move, wait to move, dwell, conditional jump and subroutine functions.

3.12.2.6. The modules shall provide non-volatile program storage without the use of battery or super capacitor.

3.12.2.7. The follower mode shall provide either parallel or cascade operation from a single master.

3.12.2.8. The follower mode shall provide a selectable master source of encoder, analog, or internal time base.

3.12.2.9. The single axis module shall have a position loop update time of not more than 1 msec. The dual axis module shall have a position loop update time of not more than 2 msec. per axis.

3.12.3. HIGH SPEED COUNTER

3.12.3.1. A specialized high speed counter option module shall be available to accommodate applications where pulse input rates exceed the input capability of the PAC.

3.12.3.2. The high speed counter module shall provide direct processing of rapid pulse signals up to 80 KHz in frequency.

3.12.3.3. The high speed counter module shall be configurable as four independent counters counting either up or down, two independent bi-directional counters, or one counter that can calculate the difference between two changing count values.

3.13. THIRD PARTY MODULES

3.13.1. SPECIALITY I/O AND COMMUNICATIONS

3.13.1.1. Based on open architecture specifications of the vendor and explicit permission of the vendor, specialty module shall be available such as PID, Co-processor, stepper, etc.

3.13.1.2. Complete documentation, kits for building modules, and engineering resource shall be available for the 3rd party based on the type of development.

3.14. COMMUNICATIONS

3.14.1. PEER/PEER COMMUNICATIONS

3.14.1.1. A specialized option module shall be available that will allow the PAC to communicate on a token passing peer-to-peer, noise immune network providing high-speed transfer of control data.

3.14.1.2. The specialized communication module shall be configurable to broadcast data to and receive data from up to 31 other devices on a network automatically and repeatedly from a shared and dedicated database in RAM memory.

3.14.1.3. The communication medium for this specialized network shall be a high energy and noise immune single shielded twisted pair cable transmitting data at an adjustable rate of up to 153.6 Kbaud. The distance of the communication shall be up to 7500 ft at a lower baud rate.

3.14.2. MASTER/SLAVE COMMUNICATIONS

3.14.2.1. The module shall provide 3 distinct communication protocols,

3.14.2.2. There shall be a module that allows the PAC to act as a master in a communication scheme that allows the PAC to interrogate other PACs for data.

3.14.2.3. There shall be 2 ports provided on the module, thus allowing more than one task to run at the same time. The two ports can be configured as communication ports in any combination.

3.14.3. PAC AND CNC I/O INTERFACE

3.14.3.1. The I/O Interface shall provide an interface between the PAC and a CNC, allowing a CNC to control 64 I/O points on the PAC.

3.14.4. CLIENT/SERVER INTERFACE

3.14.4.1. There shall be a module that provides CLIENT/SERVER with PEER to PEER communications over Ethernet TCPIP.

3.14.4.2. Each CPU system and special module shall support up to 16 simultaneous connections.

3.15.5. Network Communications Interface Modules

3.15.5.1. Manufacture of PAC shall provide Ethernet, Profibus and DeviceNet master and slave network modules. These modules shall be tightly coupled with the system including the integration of the configuration in the control software and firmware.

The controller shall be able to support up to 3 network communications modules per system of various types.